REMARKS

The present application was filed on December 21, 2001 with claims 1-20. Claims 1, 15 and 18 are the independent claims.

In the outstanding final Office Action, the Examiner raises new grounds for rejection thereby: (I) rejecting claims 1-3, 6 and 11-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,623,494 (hereinafter "Rostoker") in view of U.S. Patent No. 6,934,760 (hereinafter "Westbrook"); (ii) rejecting claim 4 under 35 U.S.C. §103(a) as being unpatentable over Rostoker and Westbrook in view of U.S. Patent No. 4,149,243 (hereinafter "Wallis"); (iii) rejecting claim 5 under 35 U.S.C. §103(a) as being unpatentable over Rostoker and Westbrook in view of U.S. Patent No. 4,593,357 (hereinafter "Ostrand"); (iv) rejecting claim 7 under 35 U.S.C. §103(a) as being unpatentable over Rostoker and Westbrook in view of U.S. Patent No. 6,058,114 (hereinafter "Sethuram"); (v) rejecting claims 8 and 9 under 35 U.S.C. §103(a) as being unpatentable over Rostoker and Westbrook in view of U.S. Patent No. 6,483,839 (hereinafter "Gemar"); and (vi) objecting to claim 12.

Regarding the objection to claim 12, Applicants have amended the dependency of claim 12 such that it now depends from independent claim 1 rather than canceled claim 10. Withdrawal of the objection is respectfully requested.

With regard to the §103(a) rejections, Applicants initially note that a proper *prima facie* case of obviousness requires that the cited references when combined must "teach or suggest all the claim limitations," and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references or to modify the reference teachings. See Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §706.02(j).

Applicants submit that the Examiner has failed to establish a proper *prima facie* case of obviousness in the §103(a) rejection of claims 1-3, 6, 11-20 over Rostoker and Westbrook, in that the Rostoker and Westbrook references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention.

Independent claim 1 is directed to a processing system comprising: first processing circuitry for performing a first function; first reassembly circuitry, associated with the first processing circuitry, for reassembling segments of received packets into reassembled packets, the segments to

be reassembled being related to the first function; first memory circuitry, associated with the first processing circuitry, for storing the packets reassembled by the first reassembly circuitry, wherein the reassembled packets stored by the first memory circuitry are used by the first processing circuitry in accordance with the first function; at least second processing circuitry for performing a second function; at least second reassembly circuitry, associated with the second processing circuitry, for reassembling at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets, the segments to be reassembled being related to the second function; and at least second memory circuitry, associated with the second processing circuitry, for storing the packets reassembled by the second reassembly circuitry, such that at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same, wherein the reassembled packets stored in the second memory circuitry are used by the second processing circuitry in accordance with the second function.

In an illustrative embodiment of the invention, packet processing system 100 is designed such that the memory required to perform the N functions is partitioned into N memories (108-1 through 108-N) which respectively provide enough bandwidth to reassemble the same data, or at least a selection of required data, to perform the corresponding function. Thus, the data may be reassembled and stored in parallel in each of the N memories. The parallel operations may be simultaneous or substantially simultaneous (e.g., delayed by some amount of time). Thus, the above-described drawbacks associated with a common, high bandwidth reassembly memory are advantageously avoided. See the specification at, for example, lines 9-15.

The Examiner in formulating the §103(a) rejection of claim 1 argues that each and every one of the above-noted limitations is met by the collective teachings of Rostoker and Westbrook. Applicants respectfully disagree.

In characterizing the Rostoker reference as allegedly meeting certain limitations of claim 1, the Examiner relies primarily on the abstract, lines 1-28; column 3, lines 34-47; column 4, lines 20-26; column 6, lines 48-67; and figure 2. However, the relied-upon portions of Rostoker fail to teach or suggest the limitations as alleged. The relied-upon portions of Rostoker state that each ATM termination unit 50 includes a processor for segmenting and reassembling the ATM cells and that each ATM terminal unit interfaces with a host unit 102. The Examiner seems to consider two of the host units to be the claimed "first processing circuitry" and "second processing circuitry," as well as the "first memory circuitry" and "second memory circuitry" Further, the Examiner seems to

consider two of the ATM terminal units to be the claimed "first reassembly circuitry" and "second reassembly circuitry."

However, even assuming this is the case for the sake of argument, no where does Rostoker disclose that the second reassembly circuitry, associated with the second processing circuitry, reassembles at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets, the segments to be reassembled being related to a second function (whereas the segments reassembled by the first reassembly circuitry are related to a first function), as recited in the independent claims. That is, no where does Rostoker state that one ATM terminal unit reassembles at least a portion of the same segments of packets reassembled by another ATM terminal unit.

The Examiner states on page 3 that "applicant does not clearly disclose if the first function and second function are distinct; so they could execute the same job/or task." However, this is not relevant to the claimed limitation. The claimed limitations recites that the second reassembly circuitry reassembles at least a portion of the same segments of packets reassembled by the first reassembly circuitry. The claim expressly recites a limitation with respect to the sameness of the packets, not the sameness of the first and second functions.

The Westbrook reference fails to supplement the above-noted deficiencies of Rostoker as applied to claim 1.

Furthermore, in characterizing the Westbrook reference as allegedly meeting certain limitations of claim 1, the Examiner relies primarily on column 7, lines 22-27 and lines 55-60, of Westbrook. However, the relied-upon portions of Westbrook fail to teach or suggest the limitations as alleged. The relied-upon portions of Westbrook appear to relate to distributed resequencing and/or reassembling components resequencing and/or reassembling packets. For example, Westbrook at column 7, lines 22-27, provides as follows:

> Moreover, these distributed resequencing and/or reassembly components 203A-N may resequence and/or reassemble a single stream of packets, or typically in a large system simultaneously resequence and/or reassemble one or more streams of packets.

In addition, Westbrook, at column 7, lines 55-60, provides as follows:

> Distributed resequencing and/or reassembly components 203A-N coordinate the resequencing and/or reassembly process(es) typically by sharing information as to what packets are currently held by each of the distributed resequencing and/or

> reassembly components 203A-N, and coordinating the sending of packets over a packet merge bus 209 (or other communications mechanism) to produce one or more streams of resequenced and/or reassembled packets.

There is no description in the relied-upon portion of Westbrook relating to, for example, the claimed features of: "at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same."

That is, while Westbrook describes multiple components for resequencing and/or reassembling packets, it is clear that Westbrook is not stating that any two components reassemble the same packets. In fact, it is clear from Figure 2A and 2b of Westbrook (and the related textual description) that Westbrook is solving the "out-of-sequence" problem (see column 1 of Westbrook) that occurs when individual packets from one or more data streams are separated so they can be individually routed on different network paths in order to get to a single destination more efficiently. Thus, distributors 200 shown in Figures 2A and 2B are understood to distribute different packets to each component 203. In fact, if the same packets could be distributed to each component (as the Examiner seems to suggest), there would be no need for the components to communicate between one another as to which packets each component received (see column 8, lines 9-11 of Westbrook).

The Rostoker reference fails to supplement the above-noted deficiencies of Westbrook as applied to claim 1.

Accordingly, it is believed that the combined teachings of Rostoker and Westbrook fail to meet the limitations of claim 1.

Also, the Examiner has failed to identify a cogent motivation for combining Rostoker and Westbrook in the manner proposed. The Examiner provides the following statement of motivation beginning at page 4, second paragraph of the Office Action:

> Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Westbrook's ideas of a plurality of reassembly components may reassemble a single stream of packets with Rostoker's system in order to provide an improved reassembling system: (Rostoker: column 3, lines 14-26).

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that

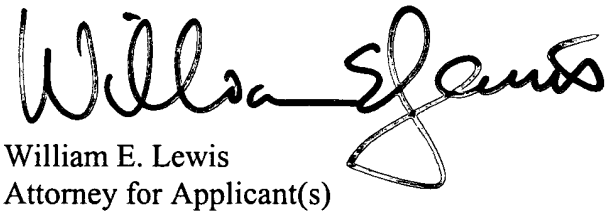
"conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. There has been no showing in the present §103(a) rejection of claim 1 of objective evidence of record that would motivate one skilled in the art to combine Rostoker and Westbrook to produce the particular limitations in question. The above-quoted statement of motivation provided by the Examiner appears to be a conclusory statement of the type ruled insufficient in the In re Sang-Su Lee case. In fact, the proposed combination appears to be based primarily on hindsight, with the Examiner attempting to reconstruct the claimed arrangement from disparate references.

Independent claims 15 and 18 include limitations similar to those of claim 1, and are therefore believed allowable for reasons similar to those described above with reference to claim 1.

Regarding the dependent claims, Applicants assert that such claims are patentable over the cited references, alone or in combination, not only for the reasons given above, but also because one or more of such claims recite patentable subject matter in their own right. Neither Wallis, Ostrand, Sethuram nor Gemar remedy the above-mentioned deficiencies.

In view of the above, Applicants believe that claims 1-9 and 11-20 are in condition for allowance, and respectfully request withdrawal of the various §103(a) rejections.

Respectfully submitted,



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